AMENDMENTS TO THE CLAIMS

Claim 1 (Currently amended): A solder bump structure and laser repair process for memory device, comprising:

providing a semiconductor wafer, which comprises a substrate, an integrated circuit, and at least one bump pad and a plurality of fuses formed on the substrate and electrically connected with the integrated circuit;

forming a first dielectric layer on a surface of the bump pad;

performing an etching process to form a contact hole in the first dielectric layer and to expose a portion of the bump pad;

forming a second dielectric layer on a surface of the semiconductor wafer outside of the contact hole;

performing an under bump metallurgy (UBM) process so as to form a metal layer on a surface of the contact hole;

forming a solder bump on the metal layer corresponding to the contact hole;

performing a circuit probing process through the solder bump and a laser repair process to cut off portions of the fuses after the formation of the solder bump, ~~and using a probing tip in~~ the circuit probing process using a probing tip ~~by~~ electrically connecting with the solder bump; and

performing a connection process to complete connection of the semiconductor wafer and a packaging board.

Claim 2 (Currently amended): The solder bump structure and laser repair process for memory device of claim

1 wherein the semiconductor wafer further comprises:

~~a plurality of fuses electrically connected with the integrated circuit;~~

at least one alignment key; and

a silicon oxide layer formed on a surface of the fuses and the alignment key.

Claim 3 (Original): The solder bump structure and laser repair process for memory device of claim 2 wherein the method of forming the second dielectric layer on the surface of the semiconductor wafer outside of the contact hole comprises:

forming the second dielectric layer on the surface of the semiconductor wafer; and

performing a photo-etching-process (PEP) to remove portions of the second dielectric layer formed on the surface of the contact hole, the fuses, and the alignment key.

Claim 4 (Original): The solder bump structure and laser repair process for memory device of claim 2 wherein the integrated circuit further comprises an embedded memory array.

Claim 5 (Canceled)

Claim 6 (Original): The solder bump structure and laser repair process for memory device of claim 1 wherein the second dielectric layer is composed of insulating materials such as benzocyclobutene (BCB), polyimide (PI), and BCB+PI.

Claim 7 (Currently amended) A solder bump structure and laser repair process for memory device, comprising:

providing a semiconductor wafer, which comprises a substrate, an integrated circuit, and at least one bump pad and a plurality of fuses formed on the substrate and electrically connected with the integrated circuit;

forming a dielectric layer on a surface of the bump pad;

performing an etching process to form a contact hole in the dielectric layer and to expose a portion of the bump pad;

performing an under bump metallurgy (UBM) process so as to form a metal layer on a surface of the contact hole;

forming a solder bump on the metal layer corresponding to the contact hole;

performing a circuit probing process through the solder bump and a laser repair process to cut off portions of the fuses after the formation of the solder bump, ~~and using a probing tip in~~ the circuit probing process using a probing tip ~~by~~ electrically connecting with the solder bump; and

performing a connection process to complete connection of the semiconductor wafer and a packaging board.

Claim 8 (Currently amended): The solder bump structure and laser repair process for memory device of claim 7 wherein the semiconductor wafer further comprises:

~~a plurality of fuses electrically connected with the integrated circuit;~~

at least one alignment key; and

a silicon oxide layer formed on a surface of the fuses and the alignment key.

Claim 9 (Original): The solder bump structure and laser repair process for memory device of claim 8 wherein the integrated circuit further comprises an embedded memory array.

Claim 10 (Canceled)

Claim 11 (New): A solder bump structure and laser repair process for memory device, comprising:

providing a semiconductor wafer, which comprises a substrate, an integrated circuit, and at least one bump pad and a plurality of fuses formed on the substrate and electrically connected with the integrated circuit;

forming a first dielectric layer on a surface of the bump pad;

performing an etching process to form a contact hole in the first dielectric layer and to expose a portion of the bump pad;

forming a second dielectric layer on a surface of the semiconductor wafer outside of the contact hole;

performing an under bump metallurgy process so as to form a metal layer on a surface of the contact hole;

forming a solder bump on the metal layer corresponding to the contact hole;

performing a circuit probing process through the solder bump and a laser repair process to cut off portions of the fuses after the formation of the solder bump and the second dielectric layer, the circuit probing process using a probing tip electrically connecting

with the solder bump; and

performing a connection process to complete connection of the semiconductor wafer and a packaging board.